SI Design & Measurement Principles and Best Practices

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Signal Integrity



The Tx to Rx connection:

- Digital standards refer to it as the Physical Layer or "the PHY" for short.
- Simulation tools call it the channel



Typical 100 Gbps Telecom System



Backplanes are a Critical Link









Backplane Connectors Are Advanced



Why Do I Need Signal Integrity?



What I Simulate

What I Measure



A Transparent Connector



Connector + Fixture

- 1) I should find a new job.
- 2) What is the fixture?
- 3) As-fabricated materials?
- 4) How can I tell what is wrong?
- 5) What should I fix first?

Eric Bogatin's Rule #9

Rule # 9: Never do a measurement or simulation without first anticipating what you expect to see.

- Simulations and measurements minimize risk
- Knowing what to expect saves time and money
- If you get it right you feel good
- If you get it wrong you will learn something

Signal and Power Integrity expert Eric Bogatin is the author of: Signal Integrity and Power Integrity Simplified, Prentice Hall, 2nd edition 2010



Signal Integrity Basics

- Material Loss :
 - Conductor
 - Dielectric
- Impedance Loss and S-Parameters
 - Reflections
 - Crosstalk



Frequency Dependent Channel Loss from Materials



Losses from materials:

- Dielectric loss caused by dipole movement with rapidly changing fields. Proportional to frequency.
- Conductor loss with skin effect pushing currents to lowest inductance path. Proportional to square root of frequency.



Example: Channel Loss with PCB Materials



PCB Material Loss in the Time Domain



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Real World PCB - Effective Loss Tangent

Leveraging old PCB technology

New SI requirements for the PCB fabrication document: -Glass Weave -Copper Profile -Test Structures for asfabricated PCB losses.

Pictures from Lee Ritchey of Speeding Edge, "13-TU2 Breaking the 32 Gb/s Barrier: PCB Materials, Simulations, Measurements", DesignCon2015





Design & Measure

Seminar

Via Stubs Create Capacitive Loads

How is a Via Stub Created?

- Signal current splits in two directions and sees two 50 ohm lines in parallel (25 ohms)
- Excess capacitance is created by a 25 ohm segment of equivalent circuit
- Reflections and poor signal integrity results





Backplane Data Rates are Increasing





Seminar

Impedance Reflections

"Reflections are the reality when time traveling is not allowed"



Vin does not show up instantaneously at Vout, and therefore Vin requires a round trip delay to adjust to the Vout termination. Initial Vin only sees the "characteristic impedance" Zo.



Telegrapher's Equations



Voltages and Currents are changing with Time and Distance (Magnitude and Phase)



- Create a simple model of a transmission line.
- Utilize calculus to analyze the model when summing a series of incremental length sections.

Oliver Heaviside 1850-1925

For small R and G

$$\frac{\partial^2}{\partial t^2} V = \frac{1}{LC} \frac{\partial^2}{\partial x^2} V$$
$$\frac{\partial^2}{\partial t^2} I = \frac{1}{LC} \frac{\partial^2}{\partial x^2} I$$

<u>Sinusoidal Input</u>

$$E = E_o \cdot e^{-j\omega(\frac{x}{c} - t)}$$

$$\frac{\partial^2 V(x)}{\partial x^2} + \omega^2 LC \cdot V(x) = 0$$
$$\frac{\partial^2 I(x)}{\partial x^2} + \omega^2 LC \cdot I(x) = 0$$

$$v = \frac{1}{\sqrt{LC}} \qquad \qquad Z_0 = \sqrt{\frac{L}{C}}$$
$$\Gamma = \frac{Z_L - Z_S}{Z_L + Z_S}$$



Characteristic Impedance Z₀



Derivation from Telegrapher Equations:



Derivation from transmission

line charging:

Independent of Length



$$C = C_L \Delta x \quad , \quad I = \frac{\Delta Q}{\Delta t} \quad , \quad \Delta Q = CV \quad \Delta t = \frac{\Delta x}{v}$$

then $I = \frac{C_L \Delta x V}{\frac{\Delta x}{v}} = vC_L V \text{ and } Z = \frac{V}{I} = \frac{1}{vC_L}$



Time Travel is not Allowed



The Channel has finite length:

- Speed of Tx : *Signal Rise-time*
- Type of Data : Data Rate Gb/s
- Speed of Channel: *Time Delay*





Magnitude of the Reflection



Bit Rate	~1/10 th Rise Time Feature Size	High Speed Feature Size		
1 MBit	3 m (10 ft)	Matched Termination		
10 MBit	30 cm (12 in)	T-Line Zo		
100 MBit	3 cm (1.2 in)	Connector Zo		
1 GBit	3 mm (120 mils)	Passive SMT Zo		
5 GBit	0.6 mm (24 mils)	Via Zo		
10 GBit	0.3 mm (12 mils)	Die, Package, PCB Co-sim		
40 GBit	0.075 mm (6 mils)	Machining Tolerances		



Reflections from a Stub Resonator







Stub Resonator (L= $\lambda/4$)

 $L = \frac{1}{4}$ of the wavelength or electrical length p/4



Destructive Interference



Parallel Stub Resonator (L= $\lambda/4$)





Quarter-wavelength stub (L=λ/4) 1. Destructive interference 2. Virtual short

- 3. Cancellation of waves
- 4. Minimum transmission (S21)



Stub Resonator (L= $\lambda/2$)





Constructive Interference



Parallel Stub Resonator (L= $\lambda/2$)



Half-wavelength stub (L=λ/2)
1. Constructive interference
2. Virtual open
3. Addition of waves
4. Maximum transmission (S21)



Full-Path Simulation to Measurement Correlation

Parallel Stub Resonator Test Structure

J24 BALANCED : STAILE ENDED. STAIL INE SONATON

ChannelSim Embed Fixture_plus_DUT Embed DUT Fixture A Fixture B ChannelSim1 NumberOfBits=10000 ToleranceMode=Auto EnforcePassivity=yes Mode=Bit-by-bit ength=whisker I in Eye_Probe Eye_Probe1 /[1]=whisker zir R=50 Ohm Length=whisker_l in TL3 TL4 S 2 N[1]=whisker zin SingleEnded* S2P1 Length=dut_input_l in Length=dut_input_l BitRate=14 Gbps Type=Touchston Type=Touchstone W[1]=stripline_zi W[1]=stripline z in RegisterLength

10 Gb/s, PRBS9 Simulation with Full-Path MBM

SIMULATED

ADS Line-Type Model with Embedded Fixture

Measurement vs. Simulation in ADS **CMP-28 Stripline Resonator** 07 ✻ nsertion Loss -5 Simulated Data -10 Measured Data -15 -20 15 2025 30 5 10 35 40 O freq, GHz

10 Gb/s , PRBS 9



MEASURED N4951A Pattern Generator

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Circuit Model with Reflections

Scattering Parameters Behavioral Model



S-Parameters (S11, S21, S12, S22) .s2p Touchstone file



Transmission Lines are Differential



Two traces carrying complementary data, commonly used for high data rates

Why?

Receiver can reject any signal that is common to both lines

Radiation reduced (cancellation of fields)

Impedance measurements have slightly different meaning compared to single-ended measurements



Single Ended Parameters



Four-port single-ended device



Single-ended to Differential S-Parameters



Differential S-parameters



Crosstalk for Microstrip vs Stripline Analysis



Differential Standard Through Vias vs. Short Microvias



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Differential Standard Through Vias vs. Short Microvias



198.925ps

99.194 ps



Cascading S-Parameters



Simulation to Measurement Correlation "Down to the last ripple"





Do I trust the Simulation or the Measurement?



Measurement "Fixtures"

Standard coaxial SOLT Calibrations only calibrate to the end of the coaxial cable!



KEYSIGHT TECHNOLOGIES

Short Length Fixture

Can I ignore the fixture losses if I shorten the length?



What is the "Reference Plane"





Fixture Removal Benefits





Fixture De-Embedding with S-Parameters

De-Embed Simulation using S-Parameters



Output De-Embedded DUT S_Parameters



Using TDR to Verify Fixture Port 1



Using TDR to Verify Fixture Port 2

Time Domain Verifies Fixture Data Matches with the DUT Fixture





Before and After Fixture Removal



Time Domain



DUT with Fixture Removed in RED DUT with Fixture in Blue



Fixture Measurement-Based-Model (MBM)

"Model matches in the frequency and time domains"







Full Path **Embedded** Fixture + DUT Simulation



--- Model with AFR Fixture



Stellar Measurement to Simulation Correlation with Accurate Fixture Calibrations



Seminar

The Future: The Internet of Things (IOT)

More Users

Automotive Wearables IOT More Data Centers

Increased Services

Apps Security

Increased Access Rate

25GE traffic density Next Gen Data Center





Example: DDR2 Device Fixture



How to remove this fixture effect?



DDR2 Fixture De-Embedding



Scope performs de-embedding



SATA De-embedding Example





De-embedding fixture and Calibration board







Calibration Board



USB Type-C High Speed Cable Fixture



TRL Calibration Calculator							
Inputs	Er	electrical Length (cm)	Propagation Velocity		Low Phase	High Phase	
Line 1 Line 2 Line 3	3.55	6.634 1.561 0.332	1.5911E+08		30.02 30.02 30.02	150.11 150.11 150.11	
Outputs	Start Frequency (GHz)	Stop Frequency (GHz)	Time Delay (ps)	Frequency Ratio f ₂ / f ₁ >8	Line Length (mm)	PCB line length (mm)	
Short/ Open					37	37	
Load		0.200			37	37	
Thru(1x)	Thru(1x)		37	37			
Thru(2x)					74	74	
Line 1	0.200	1.000	416.96	5.00	66.343	140.343	
Line 2	0.850	4.250	98.11	5.00	15.610	89.610	
Line 3	4.000	20.000	20.85	5.00	3.317	77.317	

Calibration Structures

Through Reflect Lines (TRL)



Error Correction Techniques





High Frequency Probing

When connectors are not an option....

- PCB channel has no connectors: chip to chip.
- Direct measurement of the in-situ path is required.
- Reduced cost for repetitive production testing.





Tools and Accessories



Optical Microscope ($\sim 90 \text{ x}$ magnification)



USB Digital MICroscope ($\sim 90 \text{ x}$ magnification)



TCS60 Calibration Substrate





Mylar Tape

Fine-tip Sharpie pen

- Using a good microscope is essential.
- You might damage the probe if you cannot see its tips well.

(Make sure to use a long working range (5 cm @ 90x) microscope!)



Example GHz Probes and Probe Stations



Simultaneous Horizontal/Vertical Probing



....in Summary

"A *theory* is something nobody believes, except the person who made it. An *experiment* is something everybody believes, except the person who made it." — Albert Einstein

"A *simulation* is something nobody believes, except the person who made it. A *measurement* is something everybody believes, except the person who made it." — Paul Huray

"Always verify simulation and measurements with standards"



